CLAIMS:

1. A method of manufacturing a semiconductor device, wherein a semiconductor body is provided, at a surface, with an isolation region which is recessed in the semiconductor body, which isolation region defines a continuous active region in the semiconductor body wherein a transistor having, adjacent to the surface, emitter and collector regions of a first conductivity type and a base region of the opposite, second conductivity type are formed, said emitter, base and collector regions each being provided with a contact region, for which purpose a first silicon layer is deposited on the surface, from which silicon layer two of said three contact regions are formed, which are mutually separated by an intermediate region wherein the first semiconductor layer is removed, which intermediate region extends transversely over the length of the active region, whereafter a second silicon layer is deposited, which is electrically insulated from the first silicon layer, and from which second silicon layer the third contact region is formed at the location of the intermediate region between the two contact regions mentioned first, characterized in that, of the two contact regions formed from the first semiconductor layer, a first contact region, which is connected to the collector region, is doped with an impurity of the first conductivity type, and the other, the second, contact region, which is connected to the base region, is doped with an impurity of the second conductivity type, the semiconductor body being doped, after the removal of the first semiconductor layer in the intermediate region, at the location of said intermediate region with an impurity of the second conductivity type to form a part of the base region which forms an intrinsic base region, after which the second semiconductor layer is deposited, from which the emitter contact and the emitter region of the first conductivity type are formed, and, in a stage after the first semiconductor layer has been removed at the location of the intermediate region and before the second semiconductor layer is deposited, strips of an electrically insulating material separating the emitter region from the isolation region are formed at two opposite sides of the active region at the location where the intermediate region between the base contact and the collector contact is adjacent to the isolation region.

2. A method as claimed in claim 1, characterized in that, prior to the deposition of the first semiconductor layer, the active region, which forms the collector of the transistor, is doped with a doping of the first conductivity type.

3. A method as claimed in claim 1 or 2, characterized in that after the formation of the intrinsic base region, a layer of an electrically insulating material is provided, which is subjected to an etching operation so as to form spacers on edges of the base contact and the collector contact, causing these contacts to be electrically insulated from the emitter contact to be formed in a subsequent stage of the production process.

4. A method as claimed in claim 3, characterized in that the spacers are embodied so as to be L-shaped.

5. A method as claimed in claim 3 or 4, characterized in that during the etching operation, parts of the layer of electrically insulating material are protected against etching by a mask in the intermediate region at the location where this intermediate region adjoins the isolation region, so that said strips of electrically insulating material separating the emitter region from the isolation region are formed by etching.

6. A method as claimed in any one of the claims 1 through 4, characterized in that the doping step carried out to form the intrinsic base region is performed prior to the provision of said strips of electrically insulating material.

7. A method as claimed in any one of the claims 1 through 6, characterized in that, if use is made of a semiconductor body of silicon, the surface of the active region is covered at the location of the intermediate region with a masking layer to form said strips of electrically insulating material, which masking layer protects the surface against oxidation and can be selectively etched with respect to silicon oxide, and said masking layer leaves parts of the active region, where strips must be formed, exposed, after which said exposed parts of the active region are provided, by means of oxidation, with a silicon oxide layer, whereafter the masking layer is removed by selective etching.

8. A method as claimed in claim 7, characterized in that the isolation region surrounding the active region is formed by means of a masked oxidation step, wherein the

active region is protected against oxidation by an oxidation mask and the unprotected region around the active region is converted to a pattern of silicon oxide which is at least partly recessed in the semiconductor body, and in a next stage of the manufacturing process, the active region is provided with said strips of silicon oxide whose thickness is smaller than that of the silicon oxide in the isolation region.

9. A method as claimed in claim 6, characterized in that, after the formation of the base contact and the collector contact, the whole is covered with a layer of an electrically insulating material from which said strips of an electrically insulating material are formed in said intermediate region by etching using a mask, after which the intrinsic base region is formed in the exposed part of the intermediate region.

10. A method as claimed in claim 4, characterized in that, before the intermediate region is defined, the semiconductor layer is covered with a dielectric layer, after which a window is formed in the dielectric layer and the first semiconductor layer, which window defines the intrinsic base region to be formed and is subsequently filled with a material which can be selectively etched with respect to the dielectric layer and the layer of an electrically insulating material to be provided hereafter, after which an etching process is carried out to form the base contact and the collector contact from the first semiconductor layer as well as the intermediate region situated between these contacts, whereafter a layer of an electrically insulating material is provided over the whole, which covers the intermediate region outside the intrinsic base region and which forms said strips of electrically insulating material along the edges of the active region, after which said material provided above the intrinsic base region is removed by means of selective etching, and the intrinsic base and the emitter are formed via the window thus obtained.

11. A method as claimed in claim 4, characterized in that the first semiconductor layer is covered with a dielectric layer, after which the base contact, the collector contact and the intermediate region situated between these contacts are formed, whereafter, in a next stage, a layer is provided of a material which can be selectively etched with respect to the dielectric layer, and which fills the intermediate region while leaving the base contact and the collector contact exposed, after which an opening is formed in this layer by means of selective etching, which opening defines the intrinsic base region and is situated at a distance

from the edges of the active region, after which the intrinsic base region and the emitter of the transistor are provided via this opening.